REMARKS

Claims 1 – 14 are pending in the present application. Applicants amend claims 1, 5, 9 and 12. No new matter is added. Support for the amendments may be found, for example, in Applicants' specification at page 8, lines 4 – 24 of Applicants' specification.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1 – 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2001/0056490 to Nagami et al. Applicants respectfully traverse this rejection.

In independent claims 1, 5, 9 and 12, Applicants disclose a packet transfer apparatus for switching and transferring a cell or frame signal between first and second nodes and a routing device. Applicants' claimed apparatus includes a switch, a memory and a shortcut controller. Applicants' shortcut controller <u>dynamically caches</u> outgoing route data transmitted by routing device to the second node over a predetermined connection path, and determines whether incoming cell or frame signals to the switch contain outgoing route information that matches to a outgoing route information cached in the memory.

If a match is found, the shortcut controller causes the switch to transfer the cell or frame signal from the first node to the second node via a shortcut and <u>without routing the cell signal via the predetermined connection path to and from the routing device</u> (see, e.g., page 8, lines 25 through 35 of Applicants' specification). If a match is not found,

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outgoing route data for the input cell is cached into the memory after being routed by the routing device through the predetermined connection path. Alternatively, Applicants' shortcut controller as claimed in claims 5 and 12 caches source data from input cells arriving at the second node for use as outgoing route information.

Nagami discloses a system for transferring IP packets over ATM networks via virtual connections, in which a router connecting two ATM networks has memory means for storing a correspondence between a virtual connection used in the network of a transmitting user and a virtual connection used in the network of the receiving user. The Examiner compares elements 203 – 206 of Nagami's router (FIG. 4) to Applicants' shortcut controller, and elements/process steps t2, t3 of Nagami's router to Applicants' cached memory.

However, Applicants' shortcut controller and memory are not <u>router elements</u> in a router comparable to the router disclosed by Nagami, but are rather <u>adjuncts of a switch 5</u> that allow switch 5 to perform shortcut processing <u>without routing a cell signal via the predetermined connection path to and from the routing device</u>. In order to accomplish this, Applicants' shortcut controller and memory effectively detect and store outgoing route data transmitted by the router to the second node over the predetermined connection path, and forward packets along the router-identified routes without <u>again</u> directly accessing the router over the predetermined connection path in order to obtain this route data.

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In addition to this fundamental architectural difference between the system of Nagami and Applicants' claimed invention, several other aspects of Applicants' claimed bypass process can be distinguished from the system disclosed by Nagami.

As illustrated in FIG. 7 of Nagami, routing tables for L3 processing (tables t2 to t4) are used for routing of frames and packets between nodes, for example, via dedicated virtual channels. The routing tables are updated by messaging (e.g., bypass pipe setup and bypass pipe release messages) between adjacent routers (see, e.g., FIG. 13 of Nagami).

In sharp contrast, Applicant's claimed invention relies monitors information for cells routed by the router associated with Applicants' switch, and dynamically caches associated information identifying output connection IDs produced by the router with a corresponding cell or frame information. Unlike the system of Nagami, standard cache algorithms employed by Applicants' claimed invention keep data current in the cache without the need for more complex messaging, and no frame assembly is needed to form L3 packets in order to determine next hop routing. As a result, bypass routing can be executed much more quickly and directly.

Nagami fails to disclose or suggest caching connection information, and in particular as claimed in Applicants' claims 5 and 12, caching output route information for cells or frames as determined from input cell signals directed from a destination node to the second node.

Accordingly, Applicants' respectfully submit that independent claims 1, 5, 9 and 12 are not made obvious by Nagami, and therefore stand in condition for allowance. As
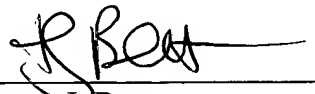
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claims 2- 4, 6 – 8, 10 – 11 and 13 – 14 respectively depend from allowable claims 1, 5, 9 and 12, Applicants respectfully submit that claims 2- 4, 6 – 8, 10 – 11 and 13 – 14 stand in condition for allowance for at least this reason.

CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that claims 1 – 14, which include independent claims 1, 5, 9 and 12 and the claims that depend therefrom, stand in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,

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